ABSTRACT

A chipset to support multiple CPU's and a layout method thereof. Those independent signal lines for delivering high frequency clock signals of the chipset are isolated from using by other signals without being multiplexed. Trace length of the independent signal line is shorter than that of the others. The spaces between the independent signal line and others are also larger than that between other signal lines. Signal transmission quality is significantly upgraded because the high frequency clock signal is not multiplexed and isolated from others.